DATA SHEET

PCK2057

70 – 190 MHz I^2C differential
1:10 clock driver

Product data
Supersedes data of 2001 May 09
File under Integrated Circuits, ICL03

2001 Jun 12

Philips
Semiconductors

PHILIPS

70 – 190 MHz I²C differential 1:10 clock driver PCK2057

FEATURES

- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications supporting DDR 200/266/300/333
- Full DDR solution provided when used with PCK2002P or PCK2002PL, and PCK2022RA
- 1-to-10 differential clock distribution
- Very low jitter (< 100 ps)
- Operation from 2.2 V to 2.7 V AV_{DD} and 2.3 V to 2.7 V V_{DD}
- SSTL_2 interface clock inputs and outputs
- HCSL to SSTL_2 input conversion
- Test mode enables buffers while disabling PLL
- Tolerant of Spread Spectrum input clock
- 3.3 V I²C support with 3.3 V V_{DD}I²C
- 2.5 V I²C support with 2.5 V V_{DD}I²C
- Form, fit, and function compatible with CDCV850

DESCRIPTION

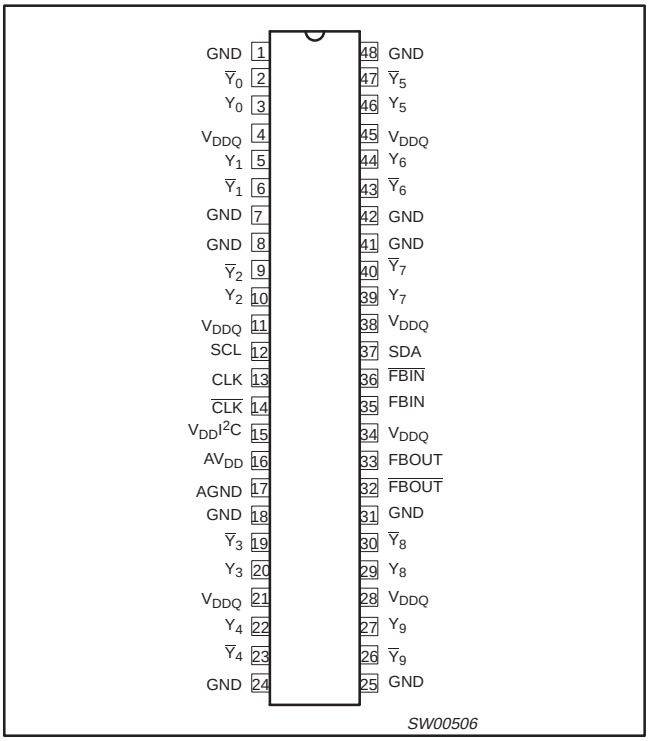
The PCK2057 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{CLK}$) to ten differential pairs of clock outputs and one differential pair of feedback clock outputs. The clock outputs are controlled by the clock inputs (CLK, $\overline{CLK}$), the feedback clocks (FBIN, $\overline{FBIN}$), the 2-line serial interface (SDA, SCL), and the analog power input (AV_{DD}). The two-line serial interface (I²C) can put the individual output clock pairs in a high-impedance state. When AV_{DD} is tied to GND, the PLL is turned off and bypassed for test purposes.

The device provides a standard mode (100 kbits) I²C interface for device control. The implementation is as a slave/receiver. The serial inputs (SDA, SCL) provide integrated pull-up resistors (typically 100 kΩ).

Two 8-bit, 2-line serial registers provide individual enable control for each output pair. All outputs default to enabled at power-up. Each output pair can be placed in a high-impedance mode, when a low-level control bit is written to the control register. The registers must be accessed in sequential order (i.e., random access of the registers is not supported). The I²C interface circuit can be supplied with either 2.5 V or 3.3 V (V_{DD}I²C).

Since the PCK2057 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power-up.

PIN CONFIGURATION



PIN DESCRIPTION

PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	Ground
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	Y_n, $\overline{Y}_n$, FBOUT, $\overline{FBOUT}$	Buffered output copies of input clock, CLK
4, 11, 21, 28, 34, 38, 45	V_{DDQ}	2.5 V supply
13, 14, 35, 36	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$	Differential clock inputs and feedback differential clock inputs
16	AV_{DD}	Analog power
17	AGND	Analog ground
37	SDA	Serial data
12	SCL	Serial clock
15	V_{DD}I²C	I²C power

ORDERING INFORMATION

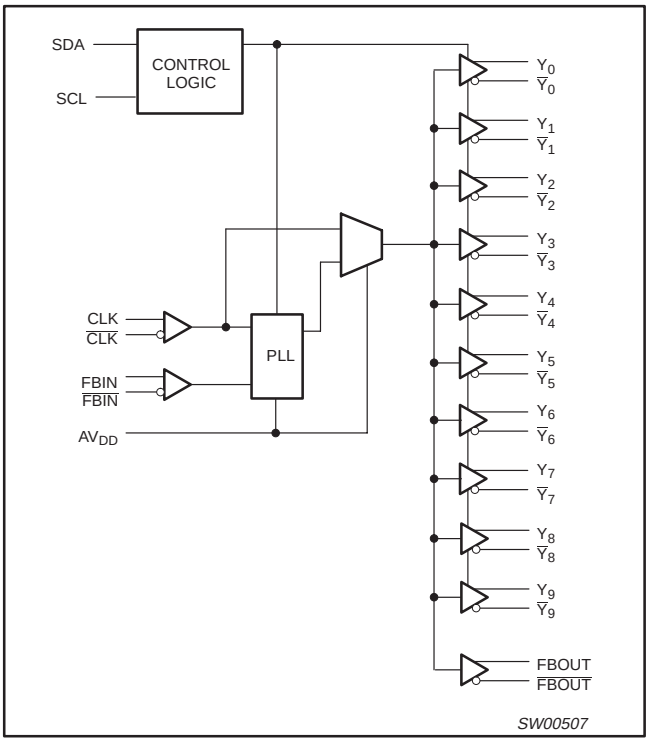
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	PCK2057DGG	SOT362-1

FUNCTION TABLE

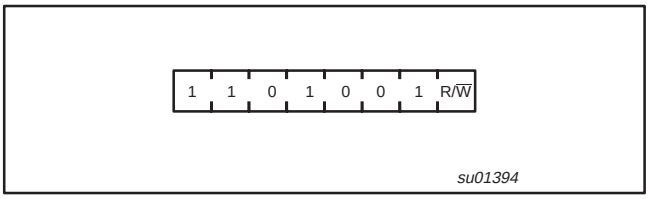
INPUTS			OUTPUTS[1]				PLL ON/OFF
AV_{DD}	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	L	H	L	H	L	H	Bypassed/OFF
GND	H	L	H	L	H	L	Bypassed/OFF
2.5 V (nom.)	L	H	L	H	L	H	ON
2.5 V (nom.)	H	L	H	L	H	L	ON

NOTES:
H = HIGH voltage level
L = LOW voltage level
1. Each output pair (except FBOUT and $\overline{FBOUT}$) can be put into a high-impedance state through the 2-line serial interface.

BLOCK DIAGRAM



I²C ADDRESS



I²C CONSIDERATIONS

I²C has been chosen as the serial bus interface to control the PCK2057. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I²C devices.

1) Address assignment: The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	1	0	1	0	0	1	0

NOTE: The R/$\overline{W}$ bit is used by the I²C controller as a data direction bit. A ‘zero’ indicates a transmission (WRITE) to the clock device. A ‘one’ indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/$\overline{W}$ bit of the address will always be seen as ‘zero’. Optimal address decoding of this bit is left to the vendor.

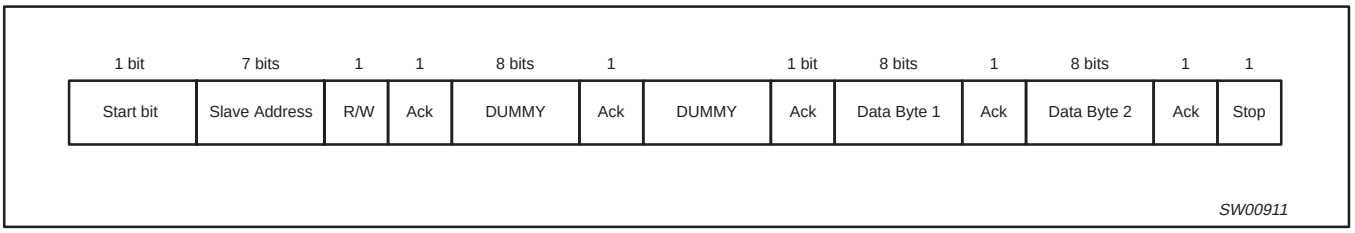
2) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

3) Logic Levels: I²C logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

4) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

5) Data Protocol: To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I²C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller “writes” to the clock driver.



NOTE: The acknowledgement bit is returned by the slave/receiver (the clock driver).

6) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I²C specification.

a) Pull-Up Resistors: Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100 kΩ is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5–6 kΩ range. Assume one I²C device per DIMM (serial presence detect), one I²C controller, one clock driver plus one/two more I²C devices on the platform for capacitive loading purposes.

(b) Input Glitch Filters: Only fast mode I²C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

For specific I²C information, consult the Philips I²C Peripherals Data Handbook IC12 (1997).

SERIAL CONFIGURATION MAP

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and "—") should be designed as "Don't Care". It is expected that the controller will force all of these bits to a "0" level.

All register bits labeled "Initialize to 0" must be written to zero during initialization. Failure to do so may result in a higher than normal operating current.

Byte 0: Active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	INITIAL VALUE	DESCRIPTION
7	2, 3	$\overline{CLK0}$, CLK0	1	Enable/Disable Outputs
6	5, 6	$\overline{CLK1}$, CLK1	1	Enable/Disable Outputs
5	9, 10	$\overline{CLK2}$, CLK2	1	Enable/Disable Outputs
4	19, 20	$\overline{CLK3}$, CLK3	1	Enable/Disable Outputs
3	22, 23	$\overline{CLK4}$, CLK4	1	Enable/Disable Outputs
2	47, 46	$\overline{CLK5}$, CLK5	1	Enable/Disable Outputs
1	44, 43	$\overline{CLK6}$, CLK6	1	Enable/Disable Outputs
0	40, 39	$\overline{CLK7}$, CLK7	1	Enable/Disable Outputs

NOTE:
1. Inactive means outputs are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Byte 1: Active/inactive register

1 = enable; 0 = disable

BIT	PIN#	NAME	INITIAL VALUE	DESCRIPTION
7	30, 29	$\overline{CLK8}$, CLK8	1	Enable/Disable Outputs
6	27, 26	$\overline{CLK9}$, CLK9	1	Enable/Disable Outputs
5	—	—	0	Reserved
4	—	—	0	Reserved
3	—	—	0	Reserved
2	—	—	0	Reserved
1	—	—	0	Power-Down Mode Disable/Enable
0	—	—	0	HCSL Enable/Disable

NOTE:
1. Inactive means outputs are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V_{DDQ}/AV_{DD}	Supply voltage range			0.5	3.6	V
$V_{DD}I^2C$	I^2C supply voltage range			0.5	4.6	V
V_I	Input voltage range	except SCL and SDA	see Notes 2 and 3	–0.5	V_{DDQ} + 0.5	V
		SCL and SDA	see Notes 2 and 3	–0.5	$V_{DD}I^2C$ + 0.5	V
V_O	Output voltage range		see Notes 2 and 3	–0.5	V_{DDQ} + 0.5	V
I_{IK}	Input clamp current		$V_I < 0$ or $V_I > V_{DDQ}$	—	±50	mA
I_{OK}	Output clamp current		$V_O < 0$ or $V_O > V_{DDQ}$	—	±50	mA
I_O	Continuous output current		V_O = 0 to V_{DDQ}	—	±50	mA
	Continuous current to GND or V_{DDQ}			—	±100	mA
T_{stg}	Storage temperature range			–65	+150	°C

NOTES:
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 3.6 V maximum.

RECOMMENDED OPERATING CONDITIONS (see Note 1)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
	Supply voltage	V_{DDQ}		2.3	—	2.7	V
		AV_{DD}		2.2	—	2.7	V
		$V_{DD}I^2C$	see Note 2	2.3	—	3.6	V
V_{IL}	LOW-level input voltage	CLK, $\overline{CLK}$, HCSL buffer only		—	0	0.24	V
		CLK, $\overline{CLK}$		–0.3	—	V_{DDQ} – 0.4	V
		FBIN, $\overline{FBIN}$		—	—	$V_{DDQ}/2$ – 0.18	V
		SDA, SCL		—	—	$0.3 \times V_{DD}I^2C$	V
V_{IH}	HIGH-level input voltage	CLK, $\overline{CLK}$, HCSL buffer only		0.66	0.71	—	V
		CLK, $\overline{CLK}$		0.4	—	V_{DDQ} + 0.3	V
		FBIN, $\overline{FBIN}$		$V_{DDQ}/2$ + 0.18	—	—	V
		SDA, SCL		$0.7 \times V_{DD}I^2C$	—	—	V
	DC input signal voltage		see Note 3	–0.3	—	V_{DDQ} + 0.3	V
V_{ID}	Differential input signal voltage	DC: CLK, FBIN	see Note 4	0.36	—	V_{DDQ} + 0.6	V
		AC: CLK, FBIN	see Note 4	0.2	—	V_{DDQ} + 0.6	V
V_{IX}	Input differential pair cross-voltage		see Note 5	$0.45 \times (V_{IH} - V_{IL})$	—	$0.55 \times (V_{IH} - V_{IL})$	V
I_{OH}	HIGH-level output current			—	—	–12	mA
I_{OL}	LOW-level output current			—	—	12	mA
		SDA		—	—	3	mA
SR	Input slew rate		see Figure 3	1	—	4	V/ns
	SSC modulation frequency			30	—	33.3	kHz
	SSC clock input frequency deviation			0	—	–0.50	%
T_{amb}	Operating free-air temperature			0	—	+70	°C

NOTES:
1. Unused inputs must be held HIGH or LOW to prevent them from floating.
2. All devices on the I^2C-bus, with input levels related to $V_{DD}I^2C$, must have one common supply line to which the pull-up resistor is connected.
3. DC input signal voltage specifies the allowable DC execution of differential input.
4. Differential input signal voltage specifies the differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input level, and V_{CP} is the complementary input level.
5. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signals must be crossing.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input voltage	All inputs	V_{DDQ} = 2.3 V; I_I = –18 mA	—	—	–1.2	V
V_{OH}	HIGH-level output voltage		V_{DDQ} = min to max; I_{OH} = –1 mA	V_{DDQ} – 0.1	—	—	V
			V_{DDQ} = 2.3 V; I_{OH} = –12 mA	1.7	—	—	V
V_{OL}	LOW-level output voltage		V_{DDQ} = min to max; I_{OL} = 1 mA	—	—	0.1	V
			V_{DDQ} = 2.3 V; I_{OL} = 12 mA	—	—	0.6	V
		SDA	$V_{DD}I^2C$ = 3.0 V; I_{OL} = 3 mA	—	—	0.4	V
V_{OX}	Output differential cross voltage			V_{DDQ}/2 – 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V
I_I	Input current	CLK, FBIN	V_{DDQ} = 2.7 V; V_I = 0 V to 2.7 V	—	—	±10	µA
I_{OZ}	High impedance state output current		V_{DDQ} = 2.7 V; V_O = V_{DDQ} or GND	—	—	±10	µA
I_{DDPD}	Power-down current on V_{DDQ} + AV_{DD}		CLK at 0 MHz; Σ of I_{DD} and AI_{DD}	—	150	250	µA
	Power-down current on $V_{DD}I^2C$		CLK at 0 MHz; V_{DDQ} = 3.6 V	—	3	20	µA
I_{DD}	Dynamic current on V_{DDQ}		f_O = 100 MHz	—	205	230	mA
AI_{DD}	Supply current on AV_{DD}		f_O = 100 MHz	—	4	6	mA
$I_{DD}I^2C$	Supply current on $V_{DD}I^2C$		$V_{DD}I^2C$ = 3.6 V; SCL and SDA = 3.6V	—	1	2	mA
C_I	Input capacitance		V_{DDQ} = 2.5 V; V_I = V_{DDQ} or GND	2	2.8	3	pF

NOTES:
1. All typical values are at respective nominal V_{DDQ}.

TIMING REQUIREMENTS

Over recommended ranges of supply voltage and operating free-air temperature.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
f_{CLK}	Clock frequency	70	190	MHz
	Input clock duty cycle	40	60	%
	Stabilization time [1]	—	100	µs

NOTE:
1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

TIMING REQUIREMENTS FOR THE I²C INTERFACE

Over recommended ranges of operating free-air temperature and $V_{DD}I^2C$ from 3.3 V to 3.6 V..

SYMBOL	PARAMETER	STANDARD-MODE I²C-BUS		UNIT
		MIN	MAX	
f_{SCL}	SCL clock frequency	—	100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	µs
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock is generated.	4.0	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	µs
t_r	Rise time of both SDA and SCL signals	—	1000	ns
t_f	Fall time of both SDA and SCL signals	—	300	ns
$t_{SU;DAT}$	DATA set-up time	250	—	ns
$t_{HD;DAT}$	DATA hold time	0	—	ns
$t_{SU;STO}$	Set-up time for STOP condition	4	—	µs

AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PD}	Propagation delay time	Test mode/CLK to any output	—	3.7	—	ns
t_{PHL}	HIGH-to-LOW level propagation delay time	SCL to SDA (acknowledge)	—	500 [1]	—	ns
t_{en}	Output enable time	Test mode/SDA to Y output	—	85	—	ns
t_{dis}	Output disable time	Test mode/SDA to Y output	—	35	—	ns
$t_{jit(per)}$	Jitter (period); see Figure 4	100 MHz to 167 MHz	–75	—	75	ps
$t_{jit(cc)}$	Jitter (cycle-to-cycle); see Figure 5	100 MHz to 167 MHz	–75	—	75	ps
$t_{jit(hper)}$	Half-period jitter; see Figure 6	100 MHz to 167 MHz	–90	—	90	ps
$t_{\varnothing}$	Static phase offset; see Figure 1	133 MHz/V_{ID} on CLK = 0.71 V	220	—	450	ps
		167 MHz/V_{ID} on CLK = 0.71 V	140	—	270	ps
$t_{slr(o)}$	Output clock slew rate; see Figure 3	terminated with 120 Ω/14 pF	1	—	2	V/ns
$t_{sk(o)}$	Output skew; see Figure 2		—	—	75	ps
	SSC modulation frequency		30	—	33.3	kHz
	SSC clock input frequency deviation		0.00	—	–0.50	%

NOTE:
1. This time is for a PLL frequency of 100 MHz.

AC WAVEFORMS

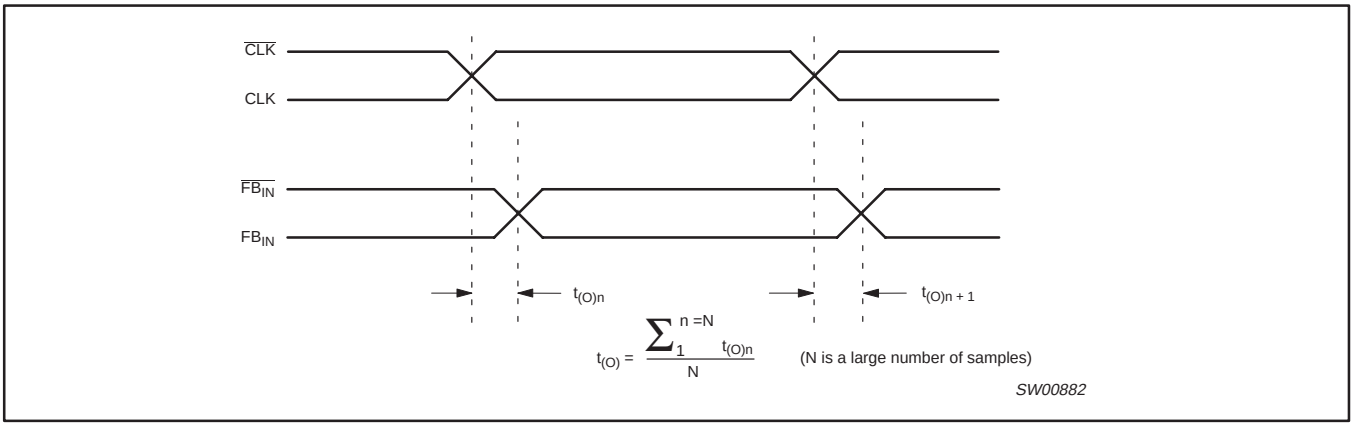


Figure 1. Static phase offset

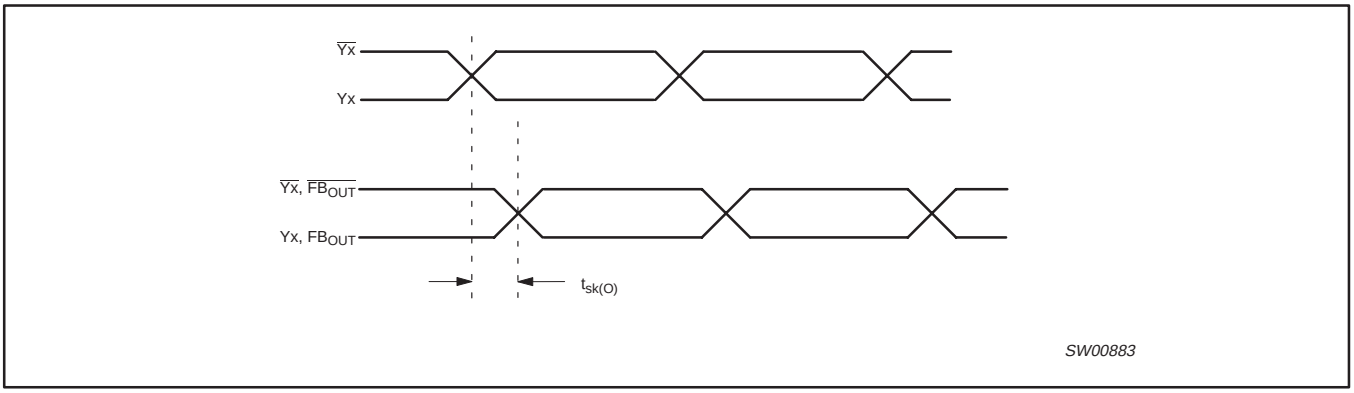


Figure 2. Output skew

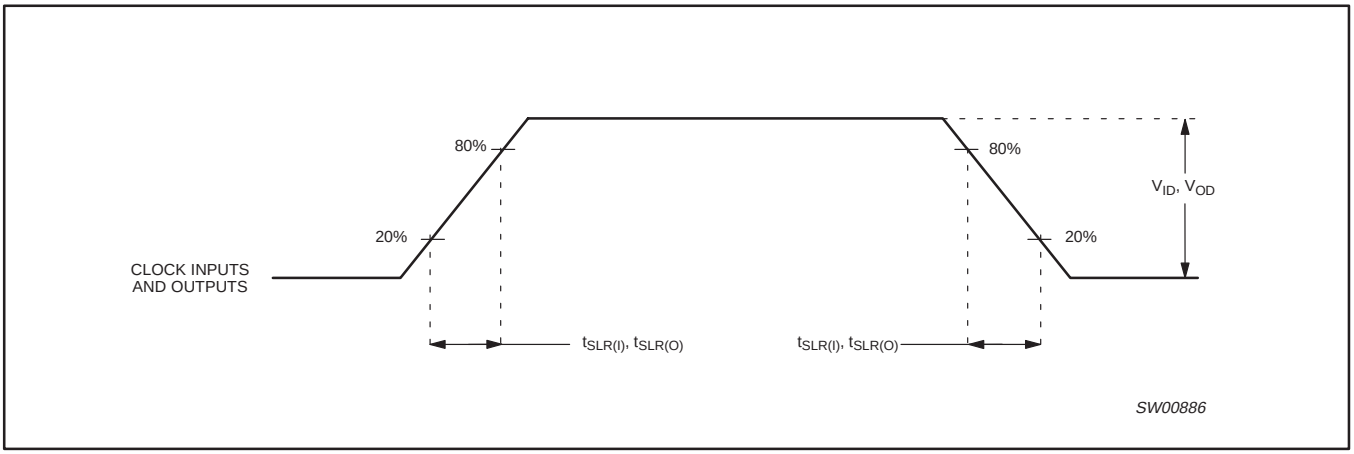


Figure 3. Input and output slew rates

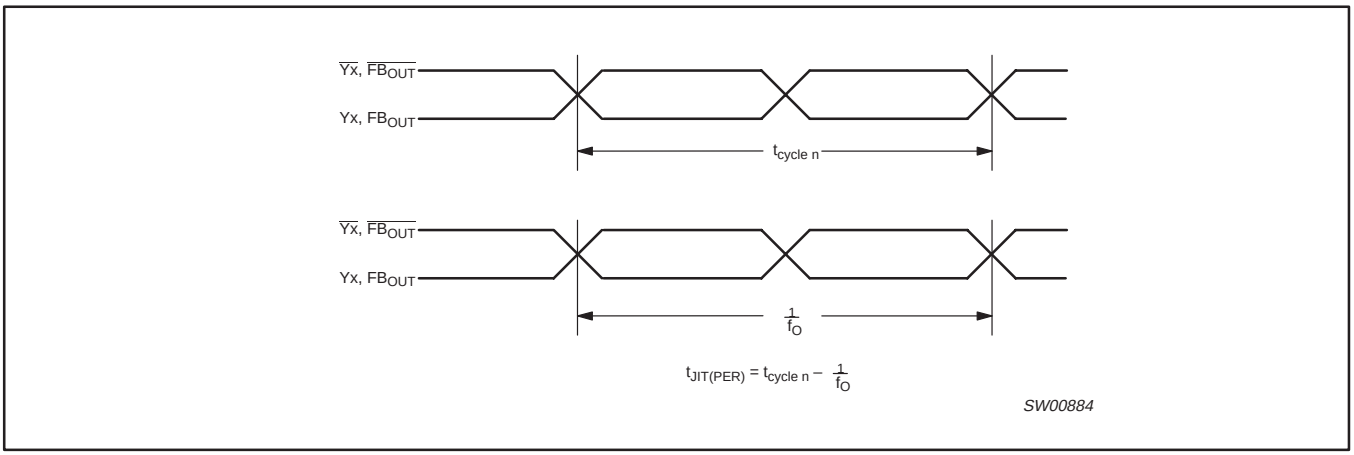


Figure 4. Period jitter

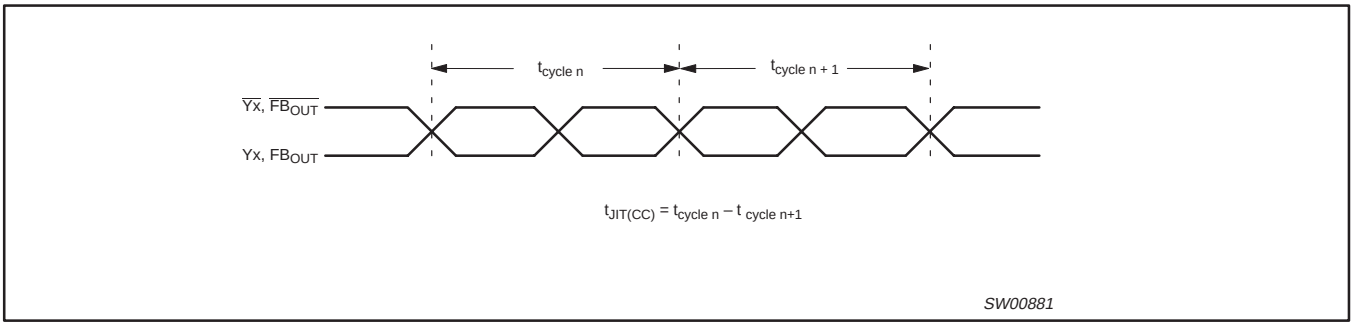


Figure 5. Cycle-to-cycle jitter

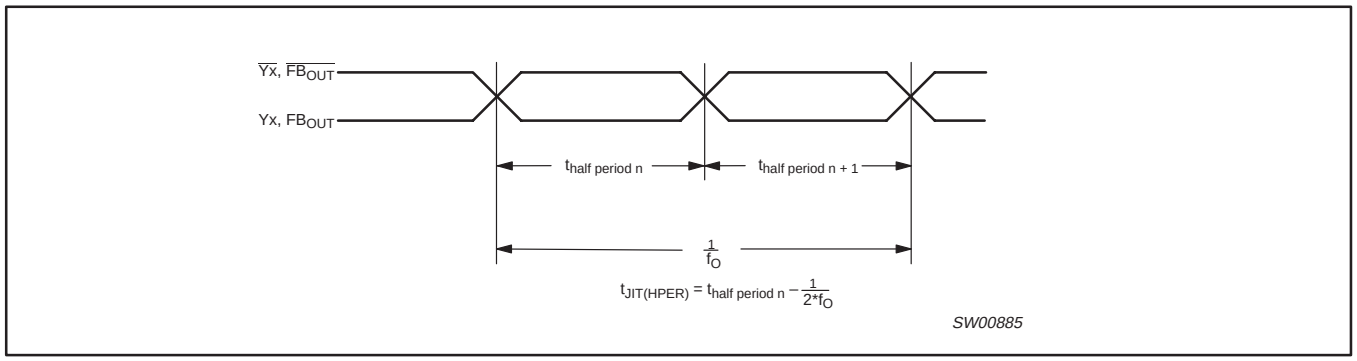


Figure 6. Half-period jitter

TEST CIRCUIT

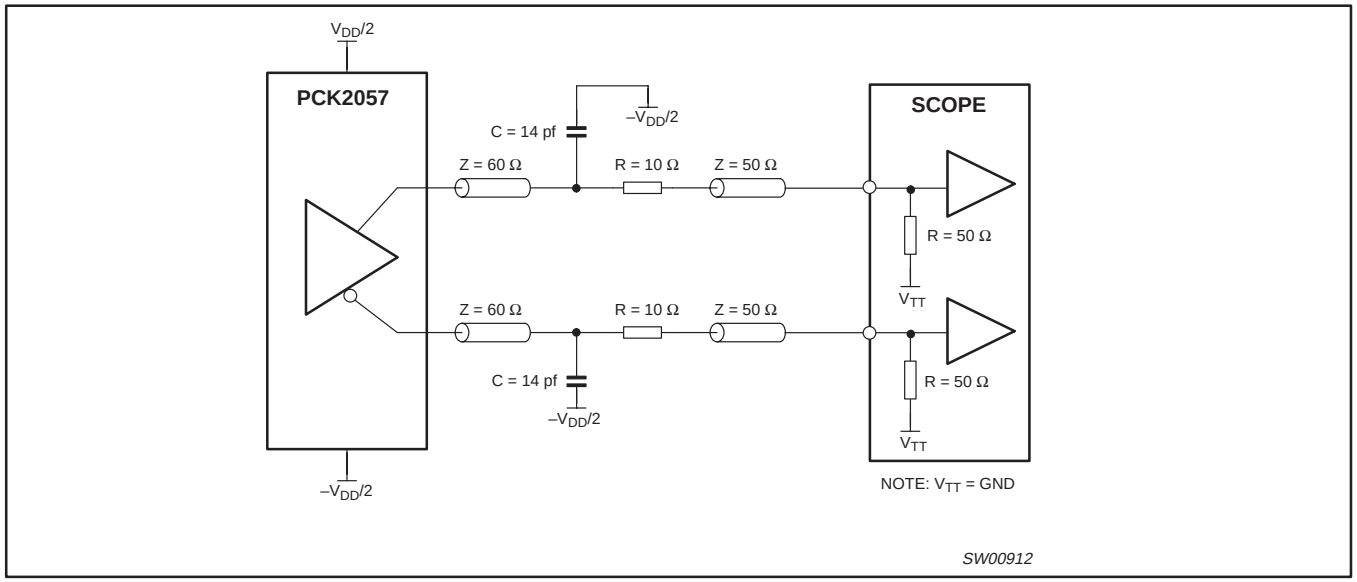
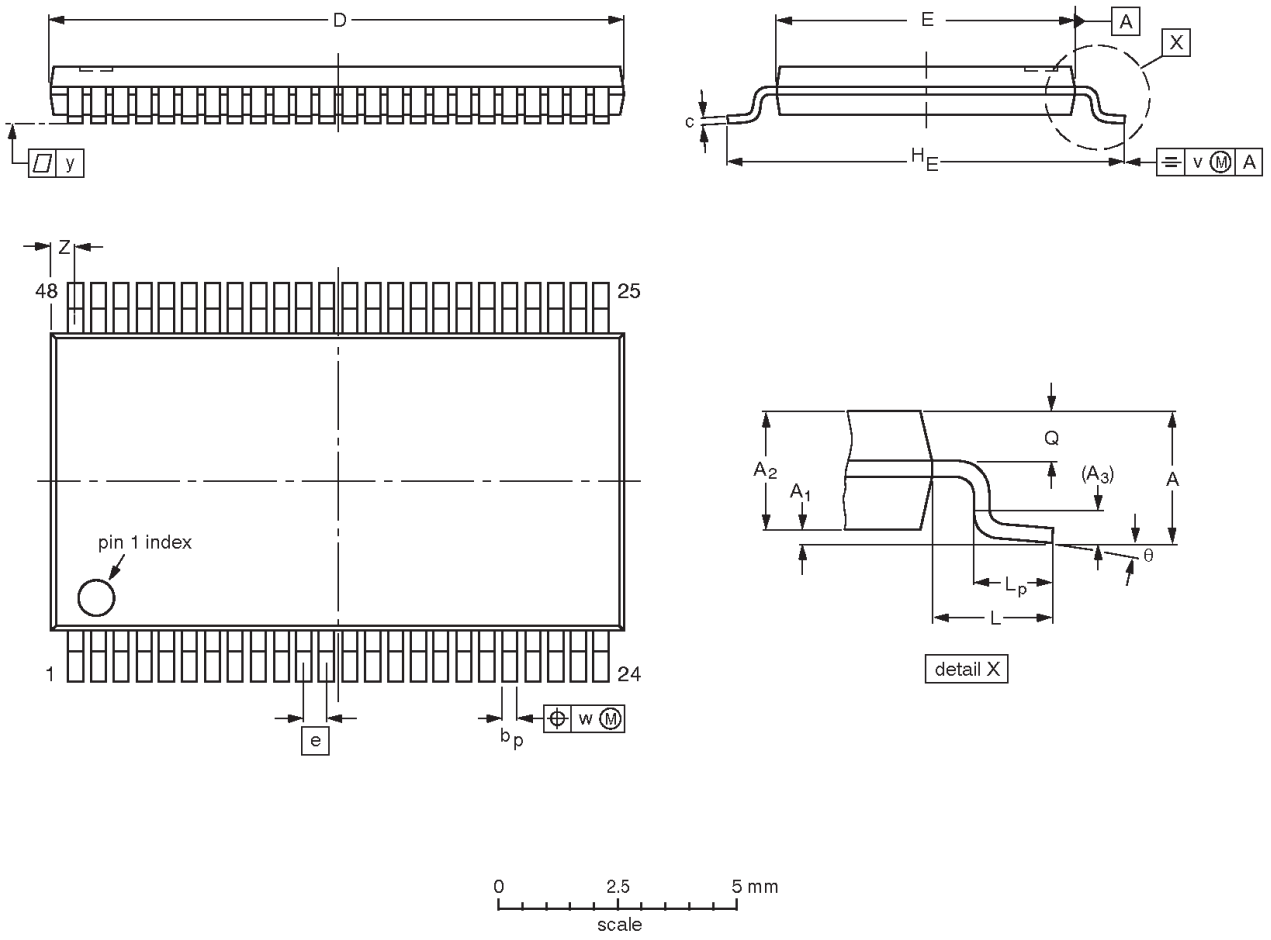


Figure 7. Output load test measurement

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

70 – 190 MHz I²C differential 1:10 clock driver PCK2057

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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